4 Digit 7-Segment Display with Serial Interface
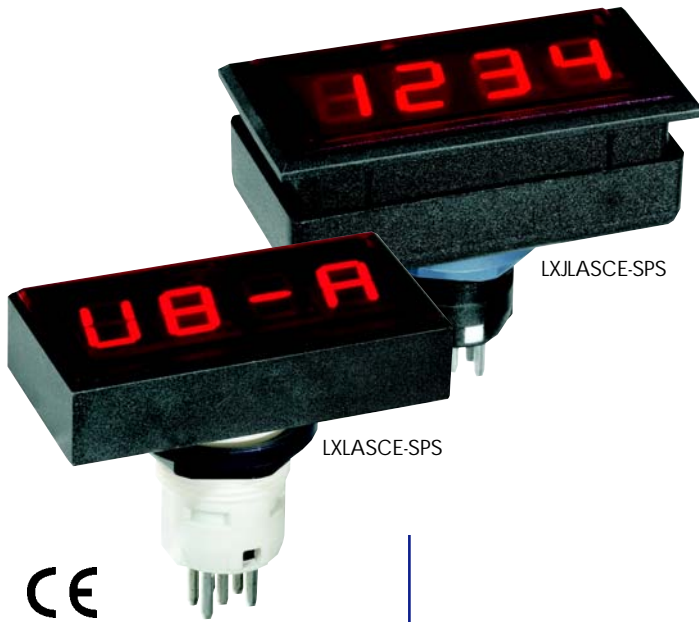
*T*his special LED display fits the QUARTRON and QUARTRON-JUWEL ranges. One of the remarkable features of the unit is that interfacing of the display is done through a serial data line. Hence, only 5 lines are necessary between output unit and display.

Characters to display

The following table indicates the characters that can be displayed as well as the relative binary code.
The decimal points are being activated through a logical 1 at the beginning of the data telegram.

LXJLASCE-SPS

LXLASCE-SPS

CE

EMV approved
Picture in original size

signs	binary code
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001
A	1010
I	1011
II	1100
U	1101
- minus	1110
blank	1111

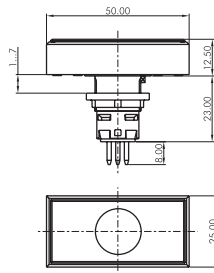## The connection

is made via a 6-pole diode plug, whose pin arrangement is shown by the following drawing:

view on the pins
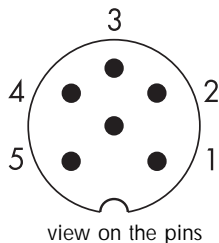
1 = Power supply
2 = Enable
3 = Clock
4 = Data
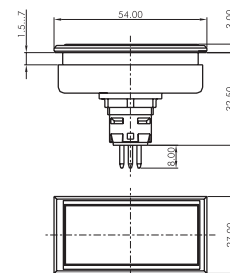5 = - (ground)

Dimensioned sketch type *LXLASCE-SPS*

50.00
12.50
23.00
8.00
25.00

Mounting hole

50.00
25.00
1.70⁺⁰·²
17.90⁺⁰·²
Ø16.20⁺⁰·²
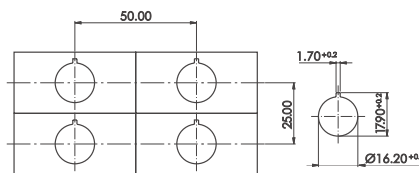
Type *LXLASCE-SPS*

Dimensioned sketch type *LXJLASCE-SPS*

1.5
7
54.00
3.00
32.50
8.00
27.00

Mounting hole

54.00
24.00
48.00
27.00

Type *LXJLASCE-SPS*

SCHLEGEL®
ELEKTROKONTAKT
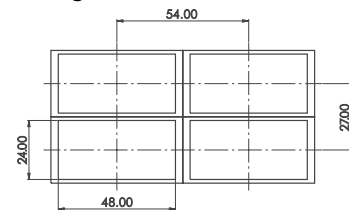
4 Digit 7-Segment Display
with Serial Interface

The data telegram must always have 20 bits. As shown in the diagram below the first bit puts (at logical 1) the decimal point after the thousand position, the second bit puts the decimal point after the hundred position, etc.
From the fifth place on follow four digits each with 4 bits.

				MSB 5	6	7	LSB 8	MSB 9	10	11	LSB 12	MSB 13	14	15	LSB 16	MSB 17	18	19	LSB 20
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
·	·	·	·	thousands digit				hundreds digit				tens digit				units digit			

Enable, Clock and Data are acting as illustrated in the diagram hereafter. When receiving data the Enable entry must be logical 0. Pay attention that data receipt is activated at the negative clock pulse.
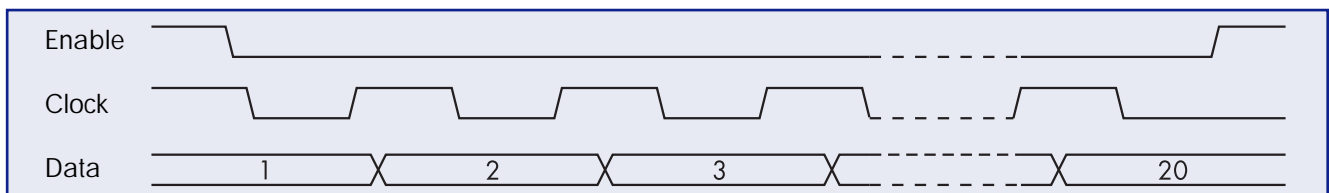
Operating instructions:
- The Enable line must always be operated. It serves for synchronization. The falling edge of Enable sets an internal scaler expecting the first bit.
- Received data is displayed immediately after receipt and handling of the 20th bit, even if the Enable line is still in Low.
- If the Enable line changes to High before having received the last bit , the display is not updated (the previous value is maintained)
- The data signal Low means logical 0, High means logical 1
- The min. clock pulse rate is "0", if necessary clock pulse and data signals can be produced manually by bounce-proof switches.

EMV instructions:
- The connecting cable must be screened from a length of 2.0 m onwards.
- The screen must be connected to ground on both sides.
- The device must be lodged into a front panel system, which is part of a tight enclosure. Before opening this housing the protective regulations of ESD must be observed. This is especially important when working at the plug connection of the device.
- A regulated power pack must be used for the power supply (e.g. SPS supply). It is not allowed to use the same circuit without additional EMC filter for switching loads.

Technical Data:
Operating Voltage:	24V DC (18-28V)
Current:	70mA at 24V
Input lines:	
Enable, Clock, Data:	24V SPS level
	Log 1 higher 6V
	Log 0 lower 3V
Operating temperature:	-30 to +70°C
Clock pulse rate:	max. 10kHz
Protection Type:	IP65
EMC:	EN 55011, EN55022, EN 50081 part 1 and 2, EN 50082 part 1 and 2

Further applications like time meter, tacho 1/min, up- and down-counter and customized signs upon request.